4K RAM BOARD

DOCUMENTATION UPDATE

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THEORY of OPERATION

88-4MCD 4K DYNAMIC RAM BOARD OPERATION

The 4K RAM Board provides 4,096 words of Dynamic Random Access Memory for the ALTAIR 8800. Each individual board contains memory protect circuitry, and address selection circuitry for any one of 16 starting address locations in increments of 4K. The maximum access time is 300 nanoseconds; thus, there is no "wait" requirement unless Refresh is occurring at the time of access.

Refresh

This memory board is designed around a dynamic integrated circuit, TMS 4030 or C2107A IC's. These dynamic IC's require each row within the chip to be accessed every 2 milliseconds or less. This is accomplished by accessing one of the 64 rows every 64 clock pulses (32 microseconds).

The Ø2 clock is buffered through one gate of IC S and then inverted through one gate of IC A. It is then divided in half through flip-flop Ta, and divided again by 16 through a 4-bit counter (IC D). The final signal is fed to the clock input of flip-flop Ga. Thus, after 32 clock pulses Ga will toggle, and will toggle again after another 32 clock pulses. This will add one count to the 6-bit counter, IC's E & F, which sets up the refresh address at the inputs of IC O.

Ga is also used to trigger single-shot Ha. This partially enables IC K pin 11 and toggles flip-flop Gb, partially enabling IC K pin 3.

If the computer is in the run mode, a SYNC pulse, inverted through one gate of IC A, will occur within approximately 10 microseconds. This causes IC K pin 11 to go low for 500 nanoseconds and IC K pin 3 to go high for 500 nanoseconds. On the falling edge of this pulse, single-shot Ia is triggered. The pulse from IC Ia pin 13 disables the machine address and triggers IC Ib. The IC Ia pin 4 output is delayed less than 100 nanoseconds and fed to the chip-enable voltage level shift circuit (4 gates of IC Z, Q1, R1, R2, D1 & C1) and also clears flip-flop Gb.

The output of this circuit provides a 500 nanosecond, +12 volt pulse to the RAM IC's to accomplish the required access.

If the machine had been in a stop mode when the refresh pulse occured, there would have been no SYNC pulse. In this case refresh would have occured with the falling edge of the pulse from IC Ha, approximately 12 microseconds later.

The function of IC Ib is to disable the read-write single-shot, IC Hb, and to pull the Ready line active if the card is accessed during refresh. This puts the machine is a wait state until refresh has been accomplished. IC Hb is then triggered for a normal read or write.

Read

IC Hb is partially enabled by MEMR. When SYNC and Ø1 occur, if refresh is not occuring keeping IC J pin 4 low, then IC K pin 8 goes low and pulls IC J pin 6 high. Approximately 90 nanoseconds later Ø1 returns low, IC K pin 8 goes high and IC J pin 6 goes low triggering IC Hb. This pulls chip enable (CE) high for 500 nanoseconds.

After approximately 300 nanoseconds the data out of the RAM chips is valid. It is latched into the 8-bit latch (IC N) via the strobe input, IC N pin 11, by IC Hb pin 5.

The final requirement to place the data onto the bus is with the latch enable inputs, pins 1 & 13 of IC N. Pin 1 is pulled low by IC J pin 8 (card select) and pin 13 is pulled high by MEMR. This enables the latch outputs and presents the data to the bus.

Write

The write mode is identical to the read mode, except that the latch outputs are not enabled and the write inputs to the RAMS are activated.

The MWRITE signal partially enables the read-write single-shot, IC Hb, and is also gated with the output of Hb to IC L pins 9 & 10. When both signals are high (active) IC L pin 8 goes low. If memory is unprotected (IC M pin 6), IC M pin 4 goes high and IC A pin 4 goes low.

This pulls the write input of the memory chips to the low active write mode while at the same time chip enable is high (Hb pin 12) and the data (buffered and inverted through IC's R & Z) is present at the RAM data inputs.

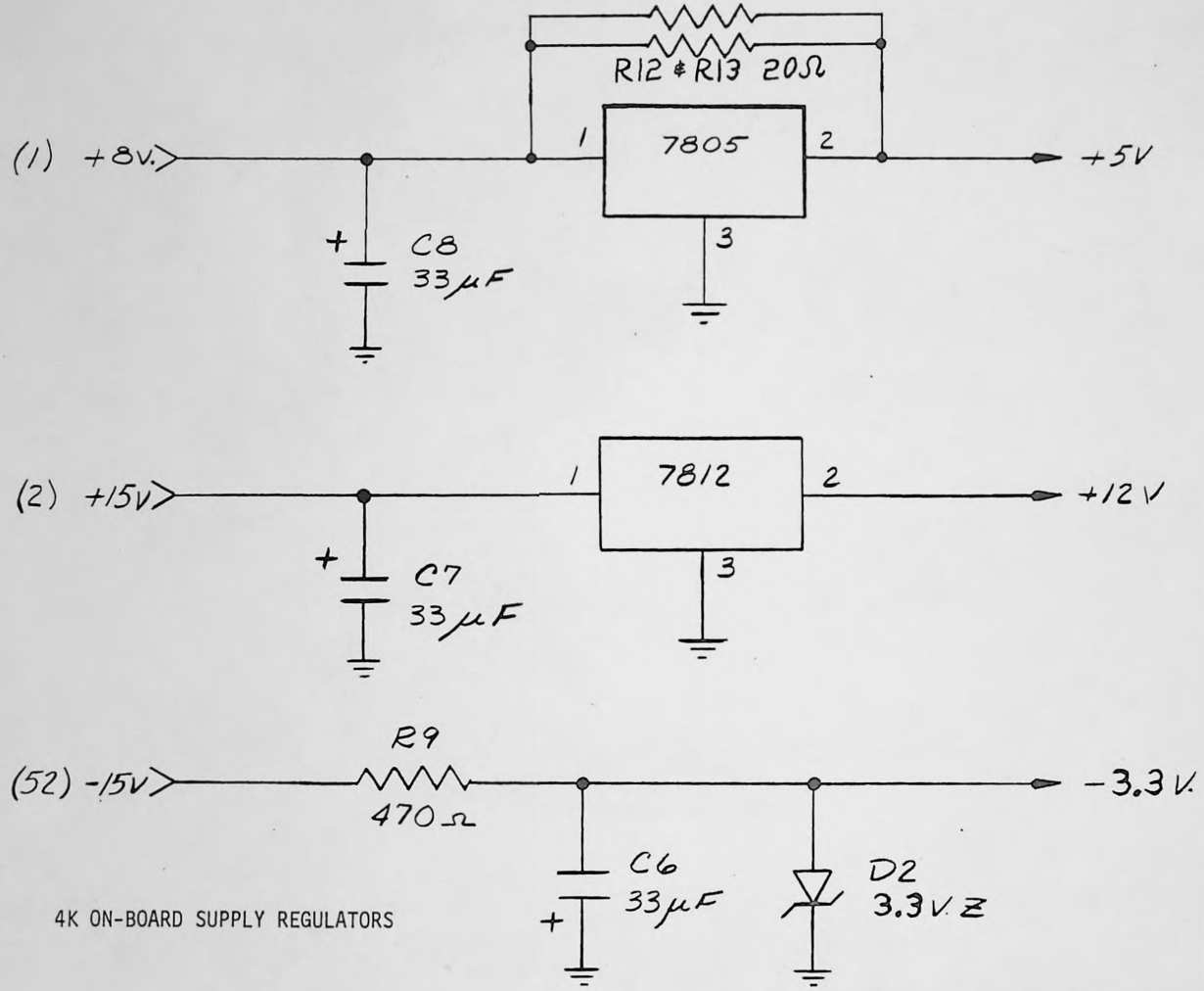
Protect

The entire 4,096 words of memory on the board can be protected via the front panel PROTECT switch.

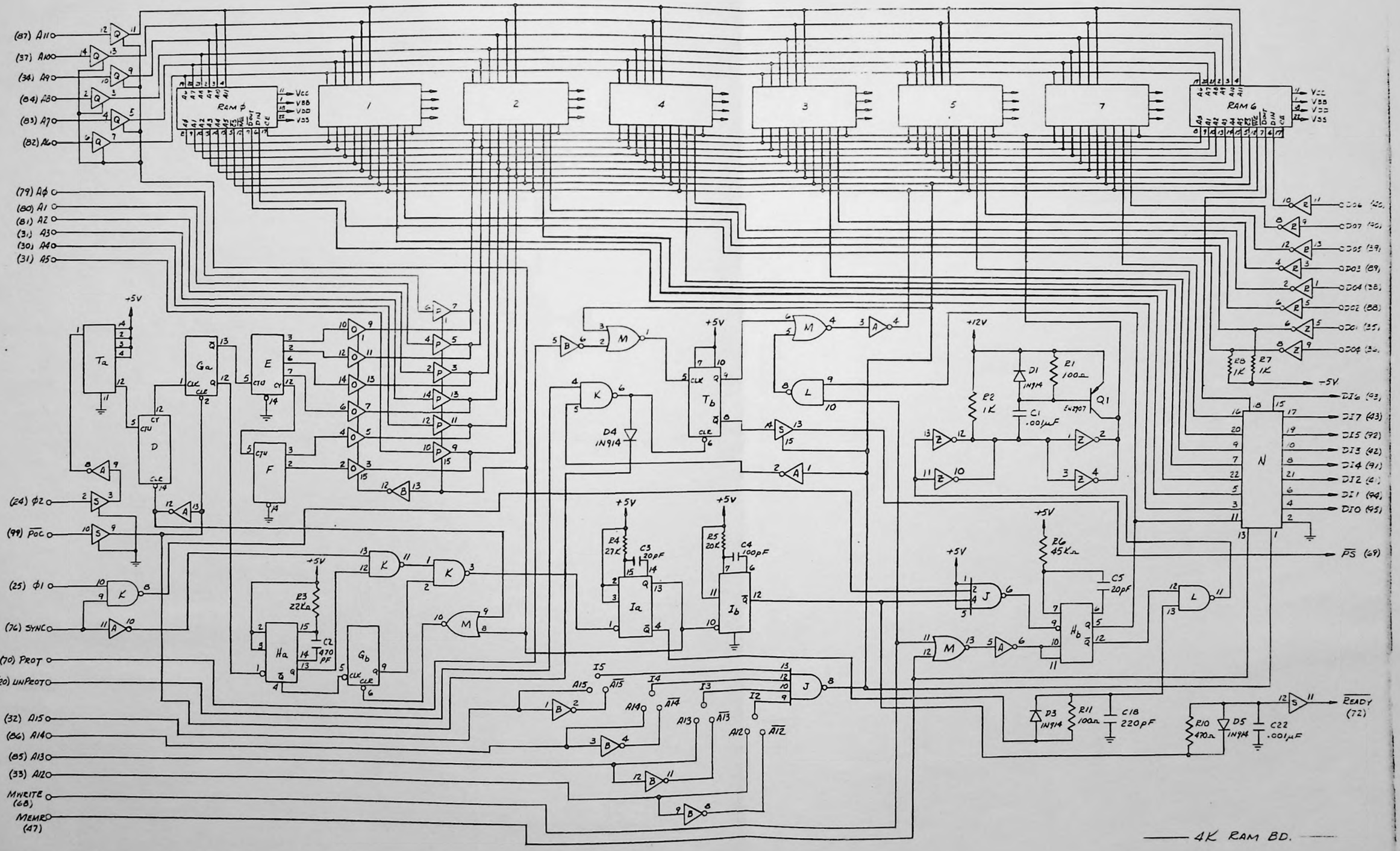
When the card is selected (IC M pin 3) and the switch lifted to the PROTECT position (IC M pin 2), the output of IC M pin 1 toggles the flip-flop Tb. This pulls IC M pin 6 high to disable the write input to the RAMS, and pulls buffer IC S pins 13 & 14 low to light the PROTECT light on the front panel.

The memory will remain protected until power is turned off or the PROTECT switch is pushed to the UNPROTECT position.

When power is first applied to the unit the $\overline{POC}$ signal (Power On Clear) is pulled low for several milliseconds, insuring that the memory is unprotected.



4K ON-BOARD SUPPLY REGULATORS


(67) A11
(37) A10
(36) A9
(84) A8
(83) A7
(82) A6
(79) A0
(80) A1
(81) A2
(31) A3
(30) A4
(31) A5
RAM 0
RAM 6
1
2
4
3
5
7
Vcc
VBB
VDD
VSS
+5V
+12V
-5V
(24) Φ2
(99) POC
(25) Φ1
(74) SYNC
(70) PROT
(20) UNPROT
(32) A15
(86) A14
(85) A13
(33) A12
MWRITE (68)
MEMR (47)
Ta
Ga
E
D
F
Gb
Ha
Hb
Ia
Ib
Tb
K
L
M
N
J
D4 IN914
D1 IN914
D3 IN914
D5 IN914
Q1 2N2907
E1 100Ω
E2 1K
E3 22KΩ
E4 27K
E5 20K
E6 1K
E7 1K
E8 45KΩ
E10 470Ω
E11 100Ω
C1 .001μF
C2 470 PF
C3 20pF
C4 100pF
C5 20pF
C18 220pF
C22 .001μF
DI6 (93)
DI7 (43)
DI5 (92)
DI3 (42)
DI4 (91)
DI2 (41)
DI1 (94)
DI0 (95)
PS (69)
READY (72)
4K RAM BD.

MEMORY ADDRESS SELECTION

There are several hardwire connections to be made on the 8800 memory boards for selecting the starting address for each board.

The starting address for each individual board is entirely optional within a few limitations. With only a single memory board in your system there is no problem, as long as the starting address selected in noted and taken into account when programming.

When more than one memory board is in the system, the sequence of starting addresses becomes critical. This is especially true when combining 1K and 4K boards in the same system. The important aspect in this case is to be sure that the individual blocks of memory on each board follow each other sequentially. There should be no gaps between the last address of one board and the starting address of the next.

The best example of this situation would be a system containing a 1K board with only 256 words of static memory together with a full 4K dynamic memory board. As may be noted from the "MEMORY ADDRESS SELECTION CHART", the starting address of the 1K boards may be selected with minimum increments of 1024 words. For the 4K board the minimum increment is 4096 words.

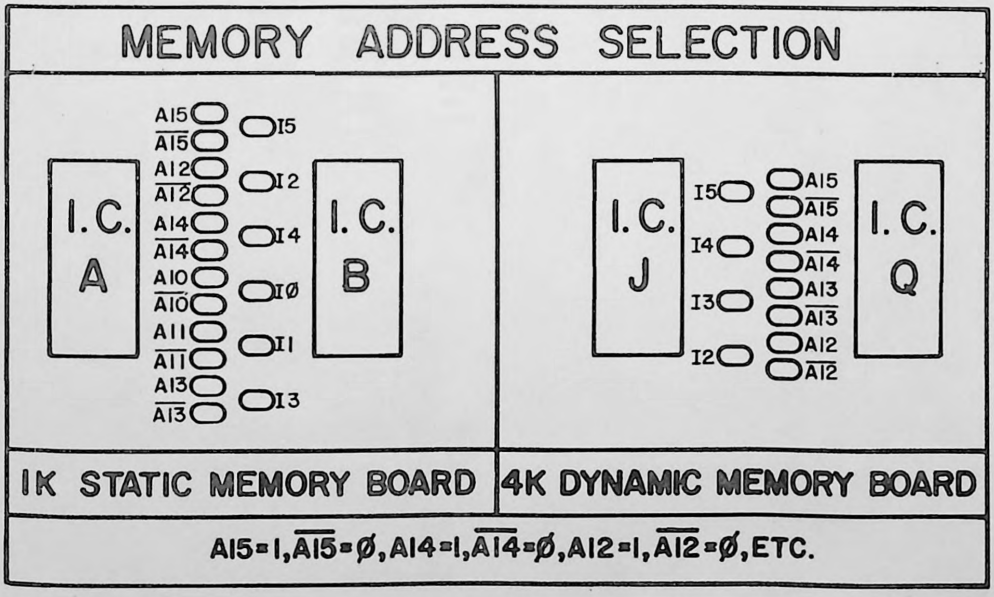
NOTE: Those addresses marked with an asterisk (*) in the chart are the possible address selections for the 4K boards, I1 & I0 being dropped for this board. Any address listed may be selected for the 1K boards.

As may be seen from studying the chart, in the example above if the 1K board is placed at an address "before" the 4K board there will be a gap of 3840 words of memory between the boards. Even with the 1K board expanded to its full 1024 words, there would still be a gap of 3072 words of memory.

In this example the 4K board address must be placed "before" the 1K board address in order to keep all possible addresses sequential. (i.e.--place the 4K board at octal address 0 and the 1K board at octal address 10 000)

The same would hold true for two 1K boards, one fully expanded and the other with only 256 words of memory. The full board must be placed first and the second board must be placed so that it follows immediately in sequence.

The chart below illustrates the address selection pads for both the 1K and the 4K memory boards. The "I" prefixed pads correspond to the "I" prefixed headings on the "MEMORY ADDRESS SELECTION CHART". The "A" prefixed pads correspond to the 1's and 0's on the "MEMORY ADDRESS SELECTION CHART" as indicated at the bottom of the chart below. The last number of the pad should always correspond in each connection. (i.e.--pad I5 must go to either A15 or $\overline{A15}$, pad I1 must go to either A11 or $\overline{A11}$)



MEMORY ADDRESS SELECTION CHART

ADDRESS LINES						ADDRESS SELECTED	
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS
0	0	0	0	0	0	0	0 *
0	0	0	0	0	1	1,024	2 000
0	0	0	0	1	0	2,048	4 000
0	0	0	0	1	1	3,072	6 000
0	0	0	1	0	0	4,096	10 000 *
0	0	0	1	0	1	5,120	12 000
0	0	0	1	1	0	6,144	14 000
0	0	0	1	1	1	7,168	16 000
0	0	1	0	0	0	8,192	20 000 *
0	0	1	0	0	1	9,216	22 000
0	0	1	0	1	0	10,240	24 000
0	0	1	0	1	1	11,264	26 000
0	0	1	1	0	0	12,288	30 000 *
0	0	1	1	0	1	13,312	32 000
0	0	1	1	1	0	14,336	34 000
0	0	1	1	1	1	15,360	36 000
0	1	0	0	0	0	16,384	40 000 *
0	1	0	0	0	1	17,408	42 000
0	1	0	0	1	0	18,432	44 000
0	1	0	0	1	1	19,456	46 000
0	1	0	1	0	0	20,480	50 000 *
0	1	0	1	0	1	21,504	52 000

ADDRESS LINES						ADDRESS SELECTED	
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS
0	1	0	1	1	0	22,528	54 000
0	1	0	1	1	1	23,552	56 000
0	1	1	0	0	0	24,576	60 000 *
0	1	1	0	0	1	25,600	62 000
0	1	1	0	1	0	26,624	64 000
0	1	1	0	1	1	27,648	66 000
0	1	1	1	0	0	28,672	70 000 *
0	1	1	1	0	1	29,696	72 000
0	1	1	1	1	0	30,720	74 000
0	1	1	1	1	1	31,744	76 000
1	0	0	0	0	0	32,768	100 000 *
1	0	0	0	0	1	33,792	102 000
1	0	0	0	1	0	34,816	104 000
1	0	0	0	1	1	35,840	106 000
1	0	0	1	0	0	36,864	110 000 *
1	0	0	1	0	1	37,888	112 000
1	0	0	1	1	0	38,912	114 000
1	0	0	1	1	1	39,936	116 000
1	0	1	0	0	0	40,960	120 000 *
1	0	1	0	0	1	41,984	122 000
1	0	1	0	1	0	43,008	124 000
1	0	1	0	1	1	44,032	126 000
1	0	1	1	0	0	45,056	130 000 *
1	0	1	1	0	1	46,080	132 000

ADDRESS LINES						ADDRESS SELECTED		
I5	I4	I3	I2	I1	I0	DECIMAL ADDRESS	OCTAL ADDRESS	
1	0	1	1	1	0	47,104	134 000	
1	0	1	1	1	1	48,128	136 000	
1	1	0	0	0	0	49,152	140 000	*
1	1	0	0	0	1	50,176	142 000	
1	1	0	0	1	0	51,200	144 000	
1	1	0	0	1	1	52,224	146 000	
1	1	0	1	0	0	53,248	150 000	*
1	1	0	1	0	1	54,272	152 000	
1	1	0	1	1	0	55,296	154 000	
1	1	0	1	1	1	56,320	156 000	
1	1	1	0	0	0	57,344	160 000	*
1	1	1	0	0	1	58,368	162 000	
1	1	1	0	1	0	59,392	164 000	
1	1	1	0	1	1	60,416	166 000	
1	1	1	1	0	0	61,440	170 000	*
1	1	1	1	0	1	62,464	172 000	
1	1	1	1	1	0	63,488	174 000	
1	1	1	1	1	1	64,512	176 000	
						Highest Directly Addressable Memory Location ⟶ 65,535	177 777	

*4K Dynamic Memory Board Selections